REMARKS

Claims 1-4, 8, 9, and 10 are pending and under consideration. Claims 1, 4, and 8 have been amended. Claims 5, 6, and 7 have been canceled herein without prejudice or disclaimer. Support for the amendments to the claims may be found in the claims as originally filed. New claims 9 and 10 have been added herein. Support for new claims 9 and 10 may be found in claims 5, 6, and 7 is filed originally, in Fig. 23, and at page 23, lines 12-30, continuing at page 24, lines 1-30, and concluding at page 25, lines 1-7 of the specification. Reconsideration is requested based on the foregoing amendment and the following remarks.

Claim Rejections - 35 U.S.C. § 102:

Claim 4 was rejected under 35 U.S.C. § 102(a) as anticipated by the section of the subject application entitled "Background Art," to which the final Office Action refers as "APAA." The rejection is traversed to the extent it would apply to the claims as amended. Reconsideration is earnestly solicited.

As provided by 35 U.S.C. §102(a):

> A person shall be entitled to a patent unless -
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.

Since the subject application, including that section of the subject application entitled "Background Art" upon which the final Office Action relies, was necessarily written *after* the invention described therein, instead of before as required by 35 U.S.C. §102(a), it is submitted that the section of the application entitled "Background Art" cannot be a valid reference against the claimed invention under the provisions of 35 U.S.C. §102(a). Withdrawal of the rejection is therefore earnestly solicited.

The second clause of claim 4, in any case, recites:

Wherein said phase comparator circuit comprises two phase comparator circuits.

The section of the subject application entitled Background Art neither teaches, discloses, nor suggests "wherein said phase comparator circuit comprises two phase comparator circuits," as recited in claim 4. The EXORs 45 and 36 shown in Fig. 3 of the subject application, rather, to which the final Office Action analogizes the recited "two phase comparator circuits," are part of a *single* phase comparator circuit.

The second clause of claim 4 recites further:

> Which perform phase comparison at every other bit of said data signals and respectively accept phases differing by one cycle (1/B sec) of said data signal to perform phase comparisons for all data signals.

The section of the subject application entitled Background Art neither teaches, discloses, nor suggests two phase comparator circuits "which perform phase comparison at every other bit of said data signals and respectively accept phases differing by one cycle (1/B sec) of said data signal to perform phase comparisons for all data signals," as recited in claim 4. Claim 4 is submitted to be allowable. Withdrawal of the rejection of claim 4 is earnestly solicited.

Claim Rejections - 35 U.S.C. § 103:

Claims 1, 2, and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the section of the subject application entitled Background Art in view of U.S. Patent No. 5,956,370 to Soda (hereinafter "Soda"). The rejection is traversed to the extent it would apply to the claims as amended. Reconsideration is earnestly solicited.

The second clause of claim 1 recites:

> A detection circuit detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern.

Neither the section of the subject application entitled "Background Art" nor Soda teach, disclose, or suggest "a detection circuit detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1. The final Office Action seeks to compensate for this deficiency with respect to the Background Art by combining the Background Art with Soda, saying at the bottom of page 5 and continuing at page 6, that:

> In analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see figure 2, component 23 and column 4, line 14 - 33).

Here, the final Office Action analogizes the recited "absence of an output of phase comparison information" to a loss of synchronization. This is submitted to be incorrect. An "absence of an output of phase comparison information," rather, means a *possibility* of the PLL losing

synchronization. This means that the loss of synchronization has not yet actually taken place, but will take place if the current state is left as it is without any control.

In Soda, moreover, the synchronism indication signal is continuously *indicative* of collapse of synchronism between the circuit input and output signals, not absent. In particular, as described at column 4, lines 22-29:

> When the synchronism indication signal is continuously indicative of collapse of synchronism between the circuit input and output signals longer than a predetermined time interval which is not shorter than the pull-in time, the oscillation control signal adjusts the oscillation frequency range in accordance with a state of the synchronism indication signal in the manner which will later be described in greater detail.

Since, in Soda, the synchronism indication signal is continuously indicative of collapse of synchronism between the circuit input and output signals, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1.

The VCO controller 23 of Soda, in fact, has a timer 51 *responsive* to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal. In particular, as described at column 5, lines 50-56:

> Referring to FIG. 4, an example of the VCO controller 23 comprises a timer 51 responsive to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal to produce a timing signal upon lapse of the predetermined time interval.

Since, in Soda, the timer 51 is responsive to the synchronism indication signal for timing the predetermined time interval from occurrence of the collapse of synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1.

Finally, in Soda, a timing counter 63 begins to count a count of the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal mentioned in the foregoing when the synchronism indication signal *indicates* occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, not when it is absent. In particular, as described at column 5, lines 50-56:

> When the synchronism indication signal indicates occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, a timing counter 63 begins to count a count of the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal mentioned in the foregoing.

Since, in Soda, a timing counter 63 begins to count a count of the pulses of the circuit input signal and produces, upon lapse of the predetermined time interval, the timing signal mentioned in the foregoing when the synchronism indication signal *indicates* occurrence of collapse of the synchronism between the circuit input signal and the voltage controlled oscillation signal or the circuit output signal, Soda is not "detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern," as recited in claim 1. Thus, even if the section of the subject application entitled Background Art were combined with Soda as proposed in the final Office Action, claim 1 would not result.

In the claimed invention, if a data signal of a certain pattern is detected, the current state is moved forcibly to a stable state where a loss of synchronization cannot occur by changing the phase of the clock signal by, for example, π radian. The detected data signal might be, for example, a data signal which is input over a long-term, and has, for example, 1500 bits. Such a data signal may cause a loss of synchronization, even though the loss of synchronization has not yet occurred. The second clause of claim 1, in particular, recites further:

> Before the occurrence of a loss of synchronization at the Phase Locked Loop (PLL) circuit.

Neither of the section of the subject application entitled "Background Art" nor Soda teach, disclose, or suggest "detecting the absence of an output of phase comparison information from said phase comparator circuit. . . before the occurrence of a loss of synchronization at the Phase Locked Loop (PLL) circuit," as recited in claim 1. In Soda, rather, a detecting circuit detects that a loss of synchronization ("collapse of synchronism") has *actually* taken place. In particular, as described at column 9, line 63-67:

> Said synchronism indication signal is continuously indicative of collapse of synchronism between said input and said output signals longer than a predetermined time interval.

Since, in Soda, a detecting circuit detects that a loss of synchronization ("collapse of synchronism") has actually taken place, Soda is not " detecting the absence of an output of phase comparison information from said phase comparator circuit. . . before the occurrence of a

loss of synchronization at the Phase Locked Loop (PLL) circuit," as recited in claim 1. Thus, even if the section of the subject application entitled Background Art were combined with Soda as proposed in the final Office Action, claim 1 would not result. Claim 1 is submitted to be allowable. Withdrawal of the rejection of claim 1 is earnestly solicited.

Claims 2 and 3 depend from claim 1 and add additional distinguishing elements. Claims 2 and 3 are thus also submitted to be allowable. Withdrawal of the rejection of claims 2 and 3 is earnestly solicited.

Allowable Subject Matter:

The Applicants acknowledge with appreciation the indication that claims 6, 7, and 8 contain allowable subject matter. New claim 9 is former claim 6 in independent form, while new claim 10 is former claim 7 in independent form. New claims 9 and 10 are thus submitted to be allowable. Claim 8 depends from claim 10 and adds further distinguishing elements. Claim 8 is thus submitted to be allowable as well.

Conclusion:

Accordingly, in view of the reasons given above, it is submitted that all of claims 1-4, 8, 9, and 10 are allowable over the cited references. Allowance of all claims 1-4, 8, 9, and 10 and of this entire application is therefore respectfully requested.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: May 13, 2008

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